A 0.35 μm CMOS 2.5 GHz Complementary $-G_M$ VCO Using PMOS Inversion Mode Varactors

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***Abstract*— A fully integrated VCO has been fabricated in a standard single poly 4-metal 0.35 μm 3.3 volt digital CMOS process, using a complementary negative G_M topology. PMOS inversion-mode varactors are used for frequency tuning. A phase noise of -97 dBc/Hz at 100 kHz offset has been measured using a single-ended test setup. The measured tuning range is 16 percent. Unbuffered and buffered versions of the oscillator were fabricated on the same die. The buffered version has an output power of nearly 0 dBm. The unbuffered core of the oscillator has a power dissipation of 35 mW.**

I. Introduction

Recently there has been an increased interest in the design of fully integrated LC VCOs using standard CMOS processes [1]–[4]. The requirements of inexpensive Bluetooth transceivers has led to the desire to integrate the 2.4 GHz RF transceiver onto the same chip with the digital data interface. In addition the low jitter requirements of high frequency digital clocks in microprocessors and high speed serial links may require the improved performance that LC oscillators can offer over traditional ring oscillators. In this paper a $-G_M$ oscillator is presented that demonstrates the feasibility of using a complementary topology in conjunction with PMOS varactors to realize a fully integrated VCO.

II. Oscillator Design

Figure 1 shows the oscillator circuit implemented in this work. This complementary structure was previously studied in [5]; it was shown that the symmetry of this circuit may lead to reduced upconversion of device 1/f noise. In [6] it was shown that the symmetry of the circuit minimizes the DC coefficient, C_0, of the impulse sensitivity function.

The complementary oscillator is essentially identical to a cross coupled pair of inverters in parallel with a tank circuit, shown in figure 2. The complementary $-G_M$ oscillator can create twice the negative resistance of its single-sided counterparts, for a given bias current, because the bias current is used in both the PMOS and NMOS devices. The negative resistance seen by the tank circuit is given by:

$$R_{negative} = -\frac{2}{G_{Mnmos} + G_{Mpmos}}. \qquad (1)$$

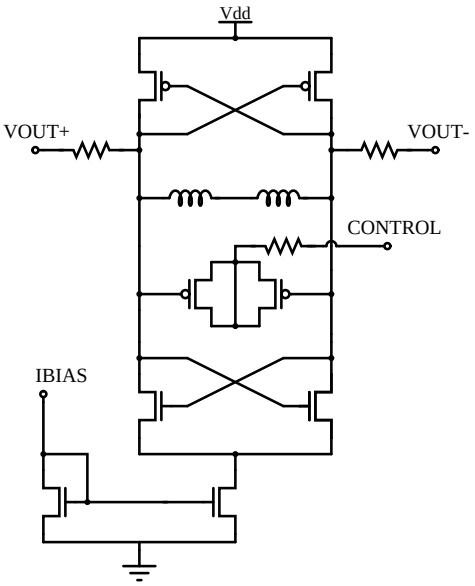

Fig. 1. Unbuffered CMOS VCO

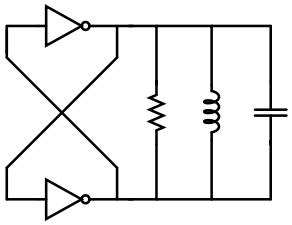

Fig. 2. Cross Coupled Inverter Oscillator

In this oscillator we used the process minimum channel length of 0.35 μm and chose the device widths to set $G_{Mnmos} = G_{Mpmos}$. This makes the PMOS and NMOS half circuits symmetric. It was found that a useful way to analyze this circuit is to de-embed the negative resistance. If the tank circuit is replaced by a test voltage source we can measure the I-V characteristic seen by the tank circuit. A simulated extracted nonlinear I-V characteristic is shown in Figure 3. This static nonlinearity was then used to simulate the oscillator in the simple parallel network shown in Figure 4. This network is completely

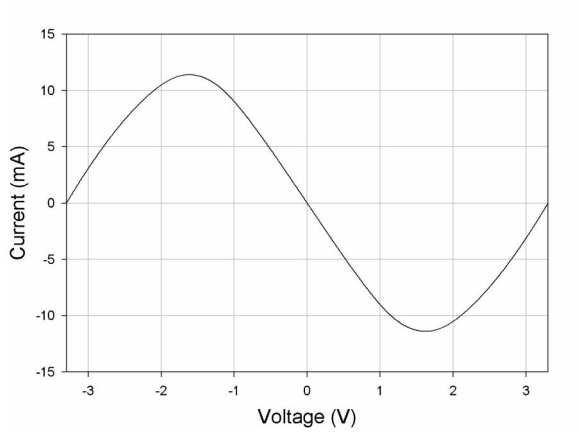

Fig. 3. Simulated I-V Characteristic of Oscillator Core

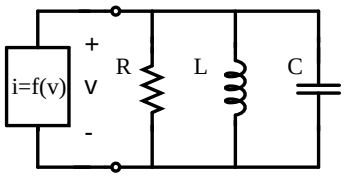

Fig. 4. Simplified Oscillator Circuit

described by the following differential equation:

$$LC\frac{d^2v}{dt^2} + \frac{L}{R}\frac{dv}{dt} + L\frac{d}{dt}f(v) + v = 0 \qquad (2)$$

Where $i = f(v)$ is the nonlinearity of figure 3. This expression can be solved numerically if a small number of harmonics is assumed. This provides a useful means of predicting oscillation amplitude and harmonic levels.

The transconductances of the devices were chosen to be 10 mS, which from (1) yields a negative resistance of $-100\,\Omega$. The total inductance of the tank was simulated to be 4.8 nH, with a quality factor of 3.4. The expected quality factor of the varactor is 30. This yields an equivalent parallel resistance of $230\,\Omega$ at 2.5 GHz. Thus the startup safety factor of the oscillator is therefore 2.3. The method of [7] can then be used to predict the phase noise of the oscillator.

$$\mathcal{L}\{\Delta\omega\} = \frac{kTR_{eff}[1+A]\left(\frac{\omega_0}{\Delta\omega}\right)^2}{V_A^2/2} \qquad (3)$$

A, the excess noise factor, is assumed equal to the startup safety factor 2.3. R_{eff}, the equivalent series resistance, is approximately $24.7\,\Omega$. V_A, the peak differential voltage amplitude, was calculated using (2) to be 2.58 V for a tank quality factor of 3.05 at 2.5 GHz. The resulting phase noise at 2.5 GHz and 100 kHz offset is -102 dBc/Hz.

Since the oscillator is essentially a pair of cross-coupled inverters, the DC level of the tank voltages will be the switching point of each inverter. This allows us to easily drive into another CMOS inverter for use as an output buffer. This buffering raises the output power to nearly 0 dBm, and should have little impact on the phase noise.

III. Inductor Design

The design of an LC monolithic VCO involves a number of tradeoffs, the most important of which is arguably the inductance value. A large value of inductance is desired in order to maximize the equivalent parallel resistance of the tank that is canceled by the negative resistance from (1). Increasing this resistance lowers the power consumption since the required transconductances become smaller. For a fixed operating frequency, increasing the inductance decreases the necessary capacitance of the tank. As the parasitic capacitances begin to dominate the tank circuit the tuning range is reduced.

This design employed simple square spiral inductors fabricated in the top layer metalization. In this 0.35 μm process, quality factors of 3-4 are typical for this structure. Others have utilized inductors consisting of multiple levels of metal or with ground shields in order to achieve a higher quality factor [8],[9]. We avoided these complex structures since they required excessive simulation time. The planar EM field solver Sonnet was used to design our inductors.

The total tank inductance consists of two 2.4 nH inductors connected in series. The use of two inductors connected in series ensures that the differential circuit is well balanced. Simulations predicted a differential Q of 3.4 for these inductors. It should be noted that substrate eddy currents produced by the magnetic coupling to the low resistivity silicon substrate represent a large portion of the total loss in this inductor. The inductor has a diameter of 220 μm, a metal width of 16 μm, and a spacing of 2 μm. The important tradeoff between ohmic loss and substrate loss as shown in [10] was considered during the inductor design. In this work the following expression for inductor Q is utilized:

$$\frac{1}{Q_{total}} = \frac{1}{Q_{metal}} + \frac{1}{Q_{substrate}} \qquad (4)$$

This expression illustrates how the series resistance and the substrate losses interact. In the design of our inductors both these factors contribute significantly to the inductor Q. The 16 μm tracewidth is a good compromise between reducing series resistance and large substrate losses, since larger area inductors have higher substrate losses due to increased coupling to the substrate.

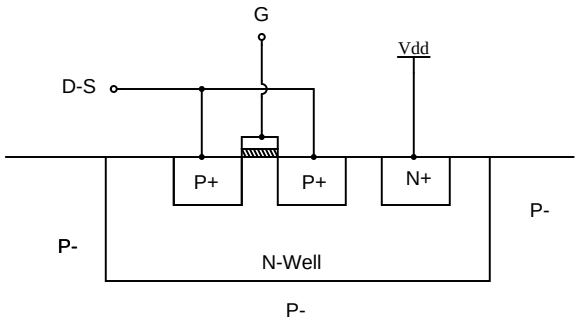

Fig. 5. PMOS Inversion Mode Varactor

IV. Varactor Design

The tunable element of this VCO is a PMOS "Inversion mode" varactor (Fig.5). This structure is identical to that of a simple PMOS transistor. This is referred to as inversion mode since the n-well is connected to V_{DD}, rather than connected to the drain-source node. The use of MOS varactor structures is discussed in detail in [11]. One advantage of the inversion mode varactor is its wide tuning range. C_{MAX}/C_{MIN} ratios of 2 are common. C_{MAX} for the varactor can be easily calculated since this is the gate to channel capacitance:

$$C_{MAX} = \frac{3.9\varepsilon_0 WL}{t_{ox}} \tag{5}$$

The varactors combined with the parasitic capacitances associated with the circuit form the total tank capacitance. Two of these PMOS varactors are connected in series and the tuning voltage is applied at the common drain-source node.

The layout of the MOS varactor is critical. The goal of layout was to minimize the resistance of the channel and the gate resistances. In order to minimize the resistance of the channel we used the minimum channel length of $0.35\,\mu$m. In order to minimize the gate resistance we use very short channel widths and connected many small devices in parallel. Additionally, we placed gate contacts on each end of the device.

V. Implementation and Measured Results

Two versions of this oscillator were fabricated. An unbuffered version of the oscillator used a resistive divider in order to drive into the $50\,\Omega$ load of the measurement equipment. $1\,\text{k}\Omega$ poly resistors are in series with the output so that each side of the differential signal is loaded by $1050\,\Omega$, which is small compared with the equivalent parallel resistance. This resistive divider attenuates the signal level a great deal and the output power of this oscillator is approximately -17 dBm. A buffered version of the oscillator was also fabricated. The measurements shown were made using the buffered version of the oscillator which has an output power of nearly 0 dBm into a $50\,\Omega$ load. These measurements are made on a single-ended basis. One half of the differential output is taken into the spectrum analyzer, while the other half was terminated into a $50\,\Omega$ precision load; in this way both sides of the circuit see similar terminations.

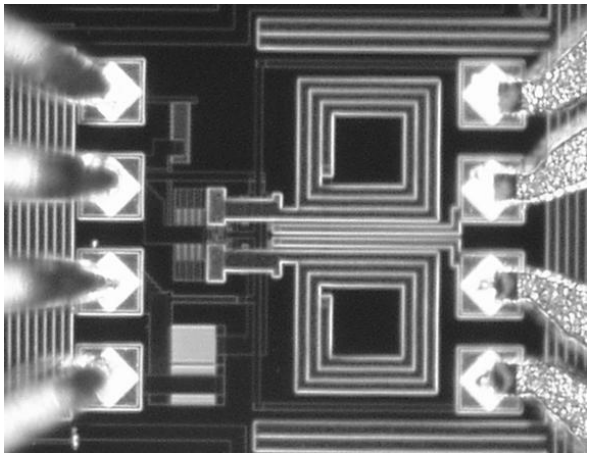

Fig. 6. Photograph of Fabricated CMOS VCO (unbuffered). The RF differential output is on the right (GSSG probe) and the DC bias probe is on the left

These circuits were tested using a Cascade probe station. The individual die were bonded to small gold plated carrier substrates for mechanical stability during probing. The fabricated unbuffered VCO, with probes in contact, is shown in figure 6. The right side of the figure shows the differential output into an Air Co-Planar GSSG probe. On the opposite side the circuit is biased through a DC probe. It was necessary to bias the VCO with batteries in order to avoid the low frequency noise that is present in many line operated power supplies. Figure 7 shows the output spectrum of the oscillator at the high end of the tuning range. The oscillator tunes 2.3-2.7 GHz for control voltages of 3.3-0 V respectively. Figure 8 shows a log plot of the output phase noise as measured using an HP8563E spectrum analyzer with a phase noise utility program. The phase noise is -97 dBc/Hz and -117 dBc/Hz at offsets of 100 kHz and 600 kHz respectively. The core of the VCO (not including the buffers) consumes approximately 35 mW at a power supply voltage of 3 V. Figure 9 shows the tuning curve of the VCO. Notice that the region on the tuning curve from 2.35 GHz to 2.65 GHz is quite linear, which makes this circuit a good choice for integrating into a PLL. The VCO gain in this linear region is approximately 240 MHz/V. The dimensions of the VCO (including $100\,\mu$m bond pads) are $700\,\mu\text{m} \times 550\,\mu\text{m}$.

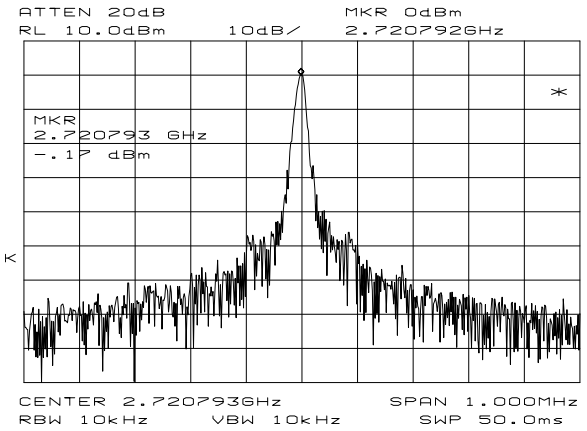

Fig. 7. Measured Buffered VCO output Spectrum, Control Voltage = 0V

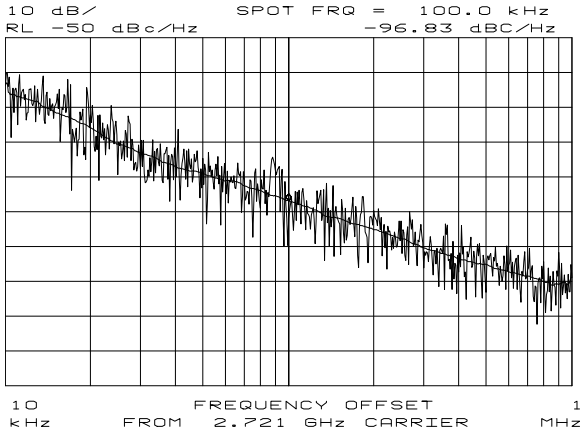

Fig. 8. Measured Buffered VCO output Phase Noise, Control Voltage = 0V

VI. Conclusions

A 2.5 GHz VCO has been implemented in a standard 0.35 μm digital CMOS process, available through the MOSIS fabrication service. The transistor models that were used were the those supplied by the MOSIS service for digital designs. This circuit clearly demonstrates the feasibility of integrating an LC VCO, even when only very low Q inductors and incomplete RF device models are available. Future work will involve testing the behavior of this VCO in a noisy mixed signal environment.

Acknowledgments

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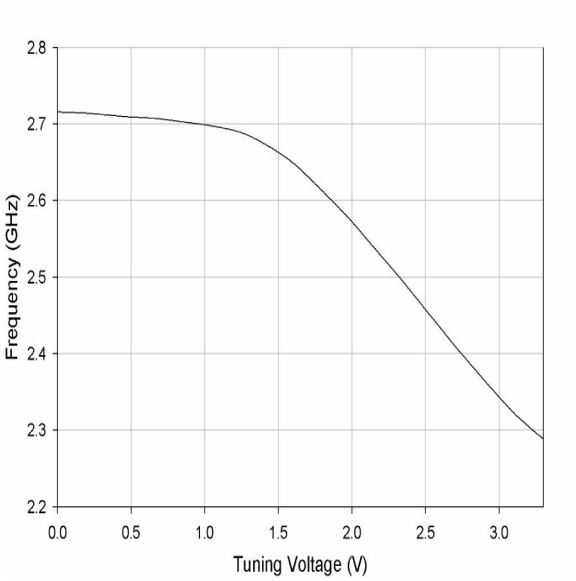

Fig. 9. Measured VCO Tuning Characteristic

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